

Amendment to the Claims:

The claims under examination in this application, including their current status and changes made in this paper, are respectfully presented.

1 (currently amended). A method for performing a write operation in a non-volatile memory system, the non-volatile memory system including a non-volatile memory having a plurality of erase units, each erase unit including a plurality of programming units arranged in a sequence, each programming unit comprising a plurality of non-volatile memory cells, wherein a first logical unit is associated with a first erase unit and includes a plurality of logical sub-units arranged in a sequence, the method comprising:

grouping the programming units within the first erase unit into a plurality of groups of programming units, the groups arranged in a sequence;

writing contents of a first logical sub-unit into a first programming unit in a first group of programming units of the first erase unit; and

then writing contents of a second logical sub-unit into a second programming unit of the first group of programming units, the second logical sub-unit later in the sequence of logical sub-units than the first logical sub-unit, and the second programming unit later in the sequence of programming units than the first programming unit; and

then writing contents of a third logical sub-unit of the first logical unit into a programming unit in a second group of programming units of the first erase unit, the third logical sub-unit earlier in the sequence of logical sub-units than the second logical sub-unit.

2 (canceled).

3 (previously presented). The method of claim 1, further comprising:

after the step of writing contents of a third logical sub-unit, writing contents of a fourth logical sub-unit into a programming unit of the second group, the fourth logical sub-unit later in the sequence of logical sub-units than the third logical sub-unit.

4 (previously presented). The method of claim 1, further comprising:

 writing a first identifier into the first group of programming units, the first identifier being arranged to substantially identify the first logical unit;

 writing contents of a first logical sub-unit of a second logical unit into a programming unit of a second group of programming units in the first erase unit; and

 writing a second identifier into the second group of programming units, the second identifier being arranged to substantially identify the second logical unit.

5 (previously presented). The method of claim 1 wherein each of the erase units is a physical block and the first logical unit is a logical block;

 wherein each of the programming units is a physical page;

 and wherein each of the logical sub-units is a logical page.

6 (original). The method of claim 5 wherein the non-volatile memory is a flash memory.

7 (original). The method of claim 6 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

8 (previously presented). The method of claim 1, wherein the contents of the third logical sub-unit substantially supercede the contents of the first logical sub-unit.

9 (canceled).

10 (previously presented). The method of claim 1 wherein the first logical sub-unit is included in a first logical grouping within the first logical unit and the third logical sub-unit is included in a second logical grouping within the first logical unit;

 and wherein the method further comprises:

 writing a first indicator into the first group of programming units that substantially identifies the first group of programming units as associated with the first logical grouping; and

 writing a second indicator into the second group of programming units that substantially identifies the second group of programming units as associated with the second logical grouping.

Claims 11 – 14 (canceled).

15 (currently amended). The non-volatile memory system of claim 22, wherein the controlling means comprises:

code devices for performing the sequence of operations; and
a processor for accessing and executing the code devices.

16 (previously presented). The non-volatile memory system of claim 22 wherein the contents of the third logical sub-unit substantially supercede the contents of the first logical sub-unit.

Claims 17 – 18 (canceled).

19 (previously presented). The non-volatile memory system of claim 22 wherein each of the erase units is a physical block and the first logical unit is a logical block;

wherein each of the programming units is a physical page;
and wherein each of the logical sub-units is a logical page.

20 (original). The non-volatile memory system of claim 19 wherein the non-volatile memory is a flash memory.

21 (original). The non-volatile memory system of claim 20 wherein the flash memory is one of a NAND flash memory and an MLC NAND flash memory.

22 (currently amended). A non-volatile memory system comprising:

a non-volatile memory having a plurality of erase units, each erase unit including a plurality of programming units arranged in a sequence, each programming unit comprising a plurality of non-volatile memory cells, wherein a first logical unit is associated with a first erase unit and includes a plurality of logical units;

means for controlling the writing of contents into the non-volatile memory according to groups of programming units within the erase units, the groups arranged in sequence, according to a sequence of operations comprising:

writing contents of a first logical sub-unit into a first programming unit in a first group of programming units of the first erase unit;

then writing contents of a second logical sub-unit into a second programming unit of the first group of programming units, the second logical sub-unit later in the sequence of logical sub-units than the first logical sub-unit, and the second programming unit later in the sequence of programming units than the first programming unit; and

then writing contents of a third logical sub-unit of the first logical unit into a programming unit in a second group of programming units of the first erase unit, the third logical sub-unit earlier in the sequence of logical sub-units than the second logical sub-unit.

Claims 23 – 42 (canceled).

43 (previously presented). The method of claim 1, further comprising:

after the step of writing contents of the third logical sub-unit, receiving contents of a fourth logical sub-unit to be written into the non-volatile memory, the fourth logical sub-unit earlier in the sequence of logical sub-units than the third logical sub-unit;

determining whether one of the groups of programming units in the first erase unit is available for writing into;

responsive to none of the groups of programming units being available for writing into, merging the contents of the first logical unit that were previously written into the plurality of programming units of the first erase unit into programming units of a first group of programming units in a second erase unit; and

then writing the contents of the fourth logical sub-unit into a programming unit of a second group of programming units of the second erase unit.

44 (previously presented). The method of claim 43, wherein the merging step merges the contents of the first logical unit that were previously written into the plurality of programming units of the first erase unit with contents of the first logical unit stored in another erase unit.

45 (previously presented). The method of claim 43, further comprising:

determining whether additional contents of the first logical unit remain to be updated;

responsive to additional contents remaining to be updated, repeating the determining, merging, and writing steps; and

responsive to additional contents not remaining to be updated, merging the contents associated with the first logical unit and stored in the second erase unit into a third erase unit.

46 (previously presented). The system of claim 22, wherein the sequence of operations further comprises:

after the operation of writing contents of the third logical sub-unit, receiving contents of a fourth logical sub-unit to be written into the non-volatile memory, the fourth logical sub-unit earlier in the sequence of logical sub-units than the third logical sub-unit;

determining whether one of the groups of programming units in the first erase unit is available for writing into;

responsive to none of the groups of programming being available for writing into, merging the contents of the first logical unit that were previously written into the plurality of programming units of the first erase unit into programming units of a first group of programming units in a second erase unit; and

then writing the contents of the fourth logical sub-unit into a programming unit of a second group of programming units of the second erase unit.

47 (previously presented). The system of claim 46, wherein the merging operation merges the contents of the first logical unit that were previously written into the plurality of programming units of the first erase unit with contents of the first logical unit stored in another erase unit.

48 (previously presented). The method of claim 46, wherein the sequence of operations further comprises:

determining whether additional contents of the first logical unit remain to be updated;

responsive to additional contents remaining to be updated, repeating the determining, merging, and writing steps; and

responsive to additional contents not remaining to be updated, merging the contents associated with the first logical unit and stored in the second erase unit into a third erase unit.